What is claimed is:

1. In an electronic system, a system for margin testing one or more components of the electronic system, comprising:

a controller internal to said electronic system; and

a digital parameter adjuster in communication with said controller and with selected ones of said components, said adjuster setting at least one operating parameter associated with at least one of said components to one or more test values in response to commands from said controller.

2. The margin testing system of claim 1, further comprising:

a hardware monitor in communication with said controller and said components to receive information from said components in response to said test values and to transmit said received information to the controller.

3. The margin testing system of claim 1, wherein said electronic system comprises:

a diagnostics software for collecting data regarding response of the electronic system to said test values of the operating parameter.

4. The margin testing system of claim 1, wherein said controller executes said diagnostics software.

5. The margin testing system of claim 1, wherein said controller transmits software command signals to said parameter adjuster to effect variation of said operating parameter.

6. The margin testing system of claim 1, wherein said operating parameter is a frequency applied to one or more of said selected components.

7. The margin testing system of claim 2, further comprising:

at least one communications bus for coupling said controller to said parameter adjuster and said hardware monitor.

8. The margin testing system of claim 1, wherein said controller implements management of said components of the electronic system.

9. The margin testing system of claim 1, wherein said controller is a Baseboard Management Controller (BMC).

10. The margin system of claim 9, wherein the BMC implements Intelligent Platform Management (IPMI) protocol.

11. The margin testing system of claim 7, further comprising:

an $I^2C$-based bus for providing communication between said BMC controller and said parameter adjuster.

12. The marging testing system of claim 11, wherein said $I^2C$-based bus is an IPMB bus.

13. The margin testing system of claim 1, wherein said parameter adjuster is a digital programmable frequency synthesizer.

14. The margin testing system of claim 13, wherein said frequency synthesizer receives an input reference clock signal and, in response to a command signal from said BMC controller, generates an output clock signal as a multiple of said input clock signal.

15. The margin testing system of claim 14, wherein said frequency synthesizer applies said output clock signal to one or more of said selected components for testing thereof.

16. The margin testing system of claim 1, wherein said electronic system comprises a computer system.

17. The margin testing system of claim 16, wherein said computer system is a computer server.

18. In a computer system, an internal system for margin testing selected components of the computer device, comprising:

a controller internal to said computer system;

a frequency control module in communication with said controller, said frequency control module varying clock frequency associated with selected ones of said components in

response to commands received from the controller for frequency margin testing of said selected components.

19. The margin testing system of claim 18, further comprising:

a voltage control module in communication with said controller, said voltage control module varying voltage applied to selected ones of said components in response to commands received from the controller for voltage margin testing of said selected components.

20. The margin testing system of claim 19, further comprising:

a fault bypass module in communication with said controller, said fault block module disabling selected automatic fault response mechanisms of said computer system in response to commands from the controller.

21. The margin testing system of claim 20, wherein said frequency control module comprises:

a frequency synthesizer generating a clock signal at a selected frequency in response to a command from the controller.

22. The margin testing system of claim 19, wherein said voltage control module comprises:

a digital potentiometer incorporated in a feedback circuit of a voltage regulator supplying voltage to said selected components so as to adjust a resistance associated with said feedback circuit in response to commands from the controller, thereby adjusting an output voltage of said regulator.

23. The margin testing system of claim 20, further comprising:

an external system in communication with said controller for transmitting commands to said controller for initiating margin testing of one or more of said components of the computer device.

24. The margin testing system of claim 23, wherein said external system comprises:

a scripting entity.

25. The margin testing system of claim 23, wherein said external system comprises:

a console providing an interface for transmitting commands from a user to said controller.

26. The margin testing system of claim 19, wherein said controller comprises:

firmware capable of being programmed to issue a sequence of commands to any of said frequency control module and said voltage control module upon receipt of a command from said external system for initiating margin testing of said selected components.

27. The margin testing system of claim 26, wherein each command of said sequence of commands causes said frequency control module to generate a selected test frequency.

28. The margin testing system of claim 26, wherein each command of said sequence of commands causes said voltage control module to generate a selected test voltage.

29. The margin testing system of claim 19, wherein said controller comprises:

a BMC.

30. The margin testing system of claim 29, further comprising:

an $I^2C$-based bus providing communication between said BMC and said frequency and voltage control modules.

31. The margin testing system of claim 30, wherein said $I^2C$-based bus is an IPMB bus.

32. The margin testing system of claim 18, wherein said computer system comprises:

a server employing an IPMI protocol.

33. The margin testing system of claim 19, further comprising:

a module for monitoring response of said computer device to any of said frequency and voltage variations.

34. The margin testing system of claim 20, wherein said frequency, voltage and fault block modules are powered by a standby power supply of said computer device when a primary power supply of said computer device is switched off.

35. A computer system, comprising

a processor;

one of more components in communication with said processor for performing a plurality of selected functions;

a controller; and

a frequency control module in communication with said controller and any of said processor and selected ones of said components, said frequency control module varying clock frequency applied to any of said processor and said selected components in response to commands from said controller so as to perform frequency margin testing thereof.

36. The computer system of claim 35, further comprising:

a voltage control module in communication with said controller and selected ones of said components requiring voltage margin testing so as to vary voltage applied thereto in response to commands from the controller.

37. The computer system of claim 36, further comprising:

a fault bypass module in communication with said controller, said fault block module disabling selected automatic fault response mechanisms of said computer system in response to commands from the controller during margin testing of any of said processor and selected ones of said components.

38. The computer system of claim 35, wherein said controller comprises:

a Baseboard Management Controller (BMC).

39. The computer system of claim 38, wherein said BMC implements Intelligent Platform Management Interface (IPMI) protocol.

40. The computer system of claim 37, further comprising:

an $I^2C$-based bus providing communications between said BMC controller and said frequency, voltage, and fault block modules.

41. The computer system of claim 40, wherein said $I^2C$-based bus is an IPMB bus.

42. The computer system of claim 37, further comprising:

a primary power source for supplying power to said computer system during normal operation of said system,

a stand-by power source for supplying power to selected components of said computer system and any of said frequency, voltage, and fault bypass modules during margin testing of said computer system, and

a power control element in communication with said controller and said primary and stand-by power supplies,

in response to commands from the controller, said power control element switching said primary power supply or stand-by power supply on or off in order to switch powering of said computer system by one power supply to the other.

43. A method for frequency margin testing of one or more marginable components of a computer system having an internal controller and a frequency control module for applying clock frequency to said marginable components, and being in communication with said controller to receive commands therefrom, comprising:

for each of a plurality of frequency test values, causing the controller to transmit a command to said frequency control module for setting an output frequency of said frequency control module to a test value, and

monitoring response of said computer system to each of said frequency test values.

44. The method of claim 43, further comprising:

utilizing a script entity to issue one or more commands to said controller in order to cause the controller to transmit one or more commands to said frequency control module to set one or more test frequencies.

45. The method of claim 44, wherein the script entity issues one command at a time to said controller..

46. The method of claim 43, further comprising:

defining a descriptor file containing a policy for use by said controller for performing margin testing.

47. The method of claim 46, wherein said descriptor file includes parameters associated with commands transmitted by said controller to said frequency control module.

48. The method of claim 43, further comprising:

executing said script entity on an external system.

49. The method of claim 48, wherein said external system is a user terminal.

50. The method of claim 43, wherein the monitoring step further comprises:

executing a diagnostics software to obtain response of the system to each of said test frequencies.

51. The method of claim 43, further comprisings:

utilizing an $I^2C$-based bus to transmit commands from said controller to said frequency control module.

52. A method for frequency margin testing of computer system having an internal controller and a frequency control module for applying clock frequency to said marginable components, and being in communication with said controller to receive commands therefrom, comprising:

programming said controller to issue a sequence of commands to said frequency control module in response to a signal for initiating frequency margin testing, each of said commands causing the frequency control module to set its output frequency to one of a plurality of frequency test values;

transmitting a signal to the controller to initiate frequency margin testing by executing said programmed sequence of commands, and

monitoring a response of the computer system to each of said frequency test values.

53. The method of claim 52, further comprising:

selecting said controller to be a BMC.

54. A method for voltage margin testing of a computer system having an internal controller and a voltage control module for applying voltages to power rails of said computer system, said voltage control module being in communication with said controller to receive commands therefrom, comprising:

for each of a plurality of voltage test values, causing the controller to transmit a command to said voltage control module for setting one of more voltages of said power rails to one or more test values; and

monitoring response of said computer system to each of said voltage test values.

55. In an electronic system, a system for margin testing one or more components of the computer system, comprising

a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system..

56. The margin testing system of claim 55, wherein said at least one of said faults corresponds to an operating parameter associated with at least one of said components crossing a selected threshold.

57. The margin testing system of claim 56, wherein said operating parameter is any of frequency, voltage or temperature.

58. The margin testing system of claim 55, further comprising:

a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said fault signals by said module.

59. The margin testing system of claim 55, wherein said fault signals comprise:

interrupt signals.

60. The margin testing system of claim 55, wherein said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system.

61. The margin testing system of claim 58, further comprising:

a hardware monitor in communication with said controller and with at least one of said components, said hardware generating an fault signal in response to occurrence of a fault associated with said at least one component.

62. The margin testing system of claim 61, wherein said hardware monitor transmits said fault signal to said fault bypass module, said fault bypass module masking said received fault signal during margin testing of said electronic device.

63. The margin testing system of claim 55, further comprising:

a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system.

64. The margin testing system of claim 63, wherein said fault bypass module masks said fault signal by intercepting said fault signal and supplying to said power control element a signal indicative of absence of a fault indicated by said fault signal.

65. The margin testing system of claim 61, wherein said at least one component is a power rail, and said hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold.

66. The margin testing system of claim 65, wherein said power control module lowers power applied to said voltage rail in response to said interrupt signal in the absence of margin testing.

67. The margin testing system of claim 55, wherein said fault bypass module comprises:

a programmable logic device programmed to provide masking of said fault signals.

68. The margin testing system of claim 61, further comprising

a temperature diode coupled to at least one of said components and said hardware monitor for measuring a temperature of said component and supplying said measured temperature to said hardware monitor.

69. The margin testing system of claim 61, wherein said fault bypass module intercepts a selected output signal of said at least one component and generates a simulated signal corresponding to said intercepted output signal for transmittal to said hardware monitor during margin testing of said component.

70. The margin testing system of claim 55, wherein said electronic system comprises a computer system.

71. The margin testing system of claim 69, wherein said computer system is a computer server.

72. The margin testing system of claim 58, wherein said controller comprises:
a BMC

73. The margin testing system of claim 72, further comprising:
a communication bus for providing communication between said BMC and said fault bypass module.

74. The margin testing system of claim 73, wherein said communication bus is an $I^2C$-based bus.

75. The margin testing system of claim 74, wherein said $I^2C$ bus is an IPMB.